of this invention to achieve unique or improved performance and reliability, particularly as to heat, power, vibration, impact, and high accelerations and decelerations.

It is also to be understood that the following claims are intended to cover all of the generic and specific features of the invention herein described, and all statements of the scope of the invention which, as a matter of language, might be said to fall therebetween.

I claim:

1. A method of making a semiconductor integrated circuit comprising:

supplying a semiconductor substrate of a first conductivity type;

supplying on top of the substrate a left and a right adjacent but laterally spaced-apart semiconductor pockets of the opposite conductivity type;

generating two PN junction regions at where the semiconductor pockets contact the substrate;

the two adjacent semiconductor pockets forming, respectively, a source and a drain regions which are spaced apart by a gap of a specified length exposing on a top surface of the substrate a gate area having the specified length; and

forming a gate layer of a substantially electrically

insulating material generally centered on the gate area;

wherein the forming step comprises forming the gate layer to have such a material and structure as to be sufficiently yieldable to minimize effects of thermal mismatch stresses between materials of the contacting substrate, pockets, and gate layer, whereby performance and reliability of the semiconductor integrated circuit is significantly improved.

2. The method as in claim 1 wherein the gate layer is yieldable without requiring appreciable amount of energy or work.

3. The method as in claim 1 including supplying a gate electrode formed of an electrically conducting material and generally centered on the gate area to control flow of electronic carriers from one of the two semiconductor pockets to the other.

4. The method as in claim 1 wherein the forming step comprises forming the gate layer by an atomic surface-smoothing process to achieve a liquid-flat surface on a lower surface of the gate layer facing the substrate.

5. The method as in claim 4 wherein the atomic surface-

smoothing process comprises:

melting the gate layer material to form a melt material; and

causing surface tension forces on the melt material to perform the atomic surface-smoothing operation; and

solidifying the atomically surface-smoothed melt material to produce the liquid-flat, solid lower gate layer surface.

6. The method as in claim 5 wherein the heating step is done by a laser beam; and

including focusing the laser beam to have such a beam size with such a power density profile as to remove a selected central top portion of the melt material to thereby form a central top concave depression on a top surface of the solidified gate layer.

7. The method as in claim 5 including stopping the laser beam heating according to a predetermined heating schedule; and

solidifying by splat cooling the remaining melt material to produce ultra-fine solidifying grains for achieving a very smooth surface on the solidified gate layer.

8. The method as in claim 5 including:

progressively solidifying the melt material from the bottom

up; and

purifying the solidifying melt material according to a phase diagram of the gate layer material, most purification taking place at the lowest layer closest to the substrate to thereby have a highest purity and electrical insulation property of the solidifying gate layer material thereat; and

when needed, remelting the solidified gate layer material and repurifying the remelted gate layer material to achieve further material purification for additional improvement in the electrical insulation property of the gate layer.

9. The method as in claim 1 wherein the forming step comprises forming the gate layer to have a curved shape for substantially reducing thermal mismatch stresses between different contacting materials through a curvature-related stress-relief mechanism.

10. The method as in claim 1 wherein the forming step comprises forming the gate layer to have a concave shape when looked from a point above the gate layer.

11. The method as in claim 1 wherein the forming step comprises forming the gate layer to have a curved shape having a radius of curvature of less than 0.5 microns.

12. The method as in claim 1 wherein the forming step comprises forming the gate layer to have a curved shape having a radius of curvature of less than 20 times thickness of the gate layer.

13. The method as in claim 1 wherein the forming step comprises forming the gate layer to have such a small thickness as to make the gate layer flexible for relieving thermal stresses between different contacting materials through flexing thereof.

14. The method as in claim 1 wherein the forming step comprises forming the gate layer to produce a gate length so small as to reduce on the gate layer at least a significant portion of thermal mismatch stresses which are proportional to the gate length.

15. The method as in claim 1 wherein the forming step comprises forming the gate layer to be of substantially the same material as materials of both the pockets and the substrate.

16. The method as in claim 1 wherein the forming step

comprises forming the gate layer to be of a material having substantially the same coefficient of thermal expansion as those of both the pockets and the substrate thereby reducing thermal mismatch stresses.

17. The method as in claim 1 wherein the gate layer has a length which is less than a length selected from the group consisting of 0.2 microns, 0.1 microns, 50 Angstroms and 10 Angstroms.

18. The method as in claim 1 wherein the gate layer is less than three to ten atomic layers thick.

19. The method as in claim 1 wherein the forming step comprises forming the gate layer to be of substantially the same material as materials of the pockets and the substrate except for no more than 10 parts per million of uncompensated dopant impurities atoms thereby reducing thermal mismatch stresses between different contacting parts.

20. The method as in claim 1 wherein the forming step comprises forming the gate layer to be of substantially the same material as materials of the pockets, the substrate, and a conductive gate electrical lead thereby reducing thermal

mismatch stresses.

21. The method as in claim 1 wherein the forming step comprises forming the gate layer to have at least a number of characteristics selected form the group consisting of: 1) having a curved shape; 2) having a sufficiently small thickness to be flexible without requiring appreciable work done thereon; 3) having a substantially same thermal coefficient of expansion as those of the substrate, the pockets, and a conductive gate electrical lead to minimize thermal mismatch stresses between different contacting parts; and 4) having a substantially same density as those of the substrate, the pockets, and a conductive gate electrical lead to minimize dynamic mismatch stresses between different contacting parts;

said number of characteristics being selected form the group consisting of two, three, and four.

22. The method as in claim 1 wherein the gate layer is metallurgically bonded, continuously and without a void visible at a magnification of over 1000 times, to the substrate with a sufficiently thick, liquid-diffusion graded bonding interfacial region therebetween to reduce thermal stress gradient across the interfacial region.

23. The method as in claim 1 wherein the gate layer is metallurgically bonded, continuously and without a void visible at a magnification of over 1000 times, to a conductive gate electrical lead with a sufficiently thick, graded bonding interfacial region therebetween.

24. The method as in claim 1 wherein the forming step comprises at least one ion-implantation step under an implanting voltage of no more than a value selected form the group consisting of 100 kilovolts, 10 kilovolts, and 1 kilovolt.

25. A semiconductor integrated circuit comprising:

a semiconductor substrate of a first conductivity type;

a left and a right adjacent but laterally spaced-apart semiconductor pockets of the opposite conductivity type and positioned on top of the substrate;

two PN junction regions at where the semiconductor pockets contact the substrate;

the two adjacent semiconductor pockets forming, respectively, a source and a drain regions which are spaced apart by a specified length thereby exposing on a top surface of the substrate a gate area;

a gate layer of a substantially electrically insulating

material generally centered on the gate area; and

a gate electrode formed of an electrically conducting material also generally centered on the gate area to control flow of electronic carriers from the source region to the drain region;

the gate layer being of such a material arranged in such a structure as to be sufficiently yieldable for minimizing effects thereon of thermal mismatch stresses between materials of the contacting substrate, pockets, gate layer, and gate electrode whereby performance and reliability of the semiconductor integrated circuit is significantly improved.

26. The semiconductor integrated circuit as in claim 25 wherein the gate layer can flex without requiring appreciable amount of energy or work.

27. The semiconductor integrated circuit as in claim 25 in which the gate layer is atomically surface-smoothed to have a liquid-flat lower surface facing the substrate.

28. The semiconductor integrated circuit as in claim 27 in which the gate layer has been in a molten state during which surface tension forces atomically surface-smooth a lower gate

surface thereof to produce the liquid-flat, lower gate layer surface facing the substrate.

29. The semiconductor integrated circuit as in claim 25 in which a central top portion of the gate layer contains a concave depression having a specified size and radius of curvature and formed by a selected precision material removal process.

30. The semiconductor integrated circuit as in claim 25 in which material of the gate layer consists essentially of a splat-cooled material containing ultra-fine grains to produce a solidified liquid-flat surface on a lower surface of the gate layer facing the substrate.

31. The semiconductor integrated circuit as in claim 25 in which material of the gate layer undergoes a phase change and is thereby significantly purified;

most purification occurring at a lowest part of the gate layer closest to the substrate to thereby have a highest electrical insulation property thereat.

32. The semiconductor integrated circuit as in claim 25 in which the gate layer has a curved shape to reduce substantially

thermal mismatch stresses through a curvature-related stress-relief mechanism.

33. The semiconductor integrated circuit as in claim 25 in which the gate layer has a concave shape when looked from a point above the gate layer.

34. The semiconductor integrated circuit as in claim 25 in which the gate layer has a curved shape having a radius of curvature of less than 0.5 microns.

35. The semiconductor integrated circuit as in claim 25 in which the gate layer has a curved shape having a radius of curvature of less than twenty times a thickness of the gate layer.

36. The semiconductor circuit as in claim 25 in which the gate layer has such a small thickness as to be sufficiently flexible to thereby relieve thermal mismatch stresses between different contacting parts through flexing thereof.

37. The semiconductor integrated circuit as in claim 25 in which the gate layer has a length which is so small as to significantly reduce thermal mismatch stresses which are

proportional to the gate length.

38. The semiconductor integrated circuit as in claim 25 in which the gate layer has no more than a length selected form the group consisting of 0.2 microns, 0.1 microns, 50 Angstroms, and 10 Angstroms.

39. The semiconductor integrated circuit as in claim 25 in which the gate layer has a thickness which is no more than two to twenty atomic layers thick.

40. The semiconductor integrated circuit as in claim 25 in which the gate layer is of substantially same material as materials of both pockets and the substrate thereby minimizing thermal mismatch stresses between different contacting parts.

41. The semiconductor integrated circuit as in claim 25 in which the gate layer is of substantially same material as materials of the pockets and the substrate, except for no more than 10 parts per million of uncompensated dopant impurities atoms thereby reducing thermal mismatch stresses between different contacting parts.

42. The semiconductor integrated circuit as in claim 25 in

which the gate layer is of substantially a same material as materials of the pockets, the substrate, and the gate electrode thereby reducing thermal mismatch stresses between different contacting parts.

43. The semiconductor circuit as in claim 25 in which the gate layer has at least a number of characteristics selected form the group consisting of: 1) having a curved shape; 2) having a sufficiently small thickness to be flexible without significant work thereon; 3) having substantially the same thermal coefficients of expansion as those of the substrate, pockets, and the conductive electrical lead to minimize thermal mismatch stresses between different contacting parts; and 4) having substantially the same density as those of the substrate, pockets, and a gate electrical lead to minimize dynamic mismatch stresses between different contacting parts;

said number being selected from the group consisting of two, three and four.

44. The semiconductor integrated circuit as in claim 25 in which the gate layer is metallurgically bonded, continuously and without a void visible at a magnification of over 1000 times, to the substrate with a graded bonding interfacial region therebetween to reduce thermal stress gradient across the

interfacial region.

45. The semiconductor integrated circuit as in claim 25 in which the gate layer is metallurgically bonded, continuously and without a void visible at a magnification of over 1000 times, to a conductive gate lead with a sufficiently thick, graded bonding interfacial region therebetween to reduce the thermal stress gradient across the interfacial region.

46. The semiconductor integrated circuit as in claim 25 in which the gate layer material has a density within 20% of that of the substrate and pockets making the circuit resistant to impacts, shocks, vibrations, and high accelerations and decelerations.

47. The semiconductor integrated device as in claim 25 in which the gate layer is formed by at least one ion-implantation step under an implanting voltage of no more than a value selected form the group consisting of 100 kilovolts, 10 kilovolts, and 1 kilovolt.

48. A method of making a semiconductor integrated circuit comprising:

providing a semiconductor substrate of a first conductivity

type;

providing on top of the substrate a semiconductor pocket of the opposite conductivity type thereby forming a PN junction region at where the semiconductor pocket contacts the substrate; and

forming a field layer of a relatively electrically insulating material starting at a top surface of the semiconductor pocket and extending substantially vertically downward to extend sufficiently deep to past the pocket and into the substrate thereby dividing the pocket into two separate parts whereby one of the two separate parts is electrically isolated from the other part by the field layer and the PN junction region;

wherein the forming step comprises forming the field layer to have such a material arranged in such a structure as to be sufficiently yieldable to minimize effects thereon of thermal mismatch stresses between materials of the substrate, pocket, and field layer whereby performance and reliability of the semiconductor device is significantly improved.

49. The method as in claim 48 wherein the forming step comprises forming the field layer to have a substantially constant thickness along its entire depth from the top surface of the semiconductor pocket down except for its bottom which is

rounded to have zero bottom width;

said field layer having a curved shape to reduce substantially thermal mismatch stresses between different contacting parts through a curvature-related stress-relief mechanism thereby minimizing defects in the field layer.

50. The method as in claim 48 wherein the forming step comprises forming the field layer to have a horizontal cross-sectional shape or boundary having a shape selected from the group consisting of a curved shape and a wave shape.

51. The method as in claim 48 wherein the forming step comprises forming the field layer to have a curved shape having a radius of curvature of less than 0.2 microns.

52. The method as in claim 48 wherein the forming step comprises forming the field layer to have a curved shape having a radius of curvature of less than twenty times a thickness of field layer.

53. The method as in claim 48 wherein the forming step comprises forming the field layer to have such a small thickness as to be flexible without requiring appreciable work thereon to appreciably relieve stresses from the field layer through

flexing thereof.

54. The method as in claim 48 wherein the forming step comprises forming the field layer to be of a material having substantially the same coefficient of thermal expansion as those of both the pocket and the substrate thereby reducing thermal mismatch stresses between the different contacting parts.

55. The method as in claim 48 wherein the forming step comprises forming the field layer to be substantially the same material as both the pocket and the substrate thereby reducing thermal mismatch stresses between the different contacting materials.

56. The method as in claim 48 wherein the forming step comprise forming the field layer to be of substantially the same material as materials of the pocket and the substrate, except for 10 parts per million of uncompensated dopant impurity atoms, thereby reducing the thermal mismatch stresses.

57. The method as in claim 48 wherein the forming step comprises forming the field layer to have at least a number of characteristics selected form the group consisting of: 1) having a curved shape; 2) having a sufficiently small thickness to be

significantly flexible without requiring appreciable work thereon; 3) having a substantially same thermal coefficients of expansion as those of the substrate and pocket to minimize thermal mismatch stresses between different contacting parts; and 4) having a substantially same density as those of the substrate and pocket to minimize dynamic mismatch stresses between different contacting parts;

said number of characteristics being selected form the group consisting of two, three, and four.

58. A laterally electrically isolated integrated circuit comprising, when viewed in a vertical cross-section:

laterally extending first and second upper semiconductor portions;

an electrically isolating region no more than 1 micron thick, and adjoining and laterally spacing from each other the upper semiconductor portions;

a lower semiconductor portion below and adjoining the electrically isolating region and the upper semiconductor portions;

a first PN junction region where the lower semiconductor portion adjoins the first upper semiconductor portion a second PN junction region where the lower semiconductor portion adjoins

the second upper semiconductor portion;

the electrically isolating region consisting essentially of an in-situ formed, substantially electrically insulating material with a rounded bottom of zero width at least at a central portion thereof, in which during the in-situ formation the isolating region introduces thermal mismatch stresses and strains into at least one of the upper and lower semiconductor portions;

the in-situ formation and rounded central bottom, in combination, allowing stress and strain relief to the semiconductor portions; and

the rounded central bottom of the isolating region being, both vertically and horizontally, sufficiently close to at least one of the PN junction regions as to significantly reduce thermal mismatch stresses and strains thereon and thereby improve performance and reliability of the integrated circuit.

59. The integrated circuit as in claim 58 in which:

the electrically isolating region consisting essentially of at least one of an oxide and a nitride.

60. The integrated circuit device as in claim 58 in which the electrically isolating layer has at least two of the following features: 1) having a thickness of no more than a

value selected from the group consisting of 0.5 microns, 0.1 microns, 100 Angstroms, and 20 Angstroms; 2) being round-bottomed; and 3) having a curved boundary on a horizontal, but not vertical, cross-section thereof to reduce the thermal mismatch strains and stresses through a curvature-related strain-relieving mechanism.

61. A method of making a semiconductor integrated circuit device comprising:

providing a semiconductor substrate of one electronic conductivity type, and having a top surface and a specified substrate density;

Providing on the top surface of the substrate a first semiconductor pocket

of an opposite electronic conductivity type and capable of supplying preselected electronic carriers of one type selected from the group consisting of electrons and holes;

providing on the top surface of the substrate at a selected lateral distance away from the first semiconductor pocket a second semiconductor pocket of the opposite electronic conductivity type and capable of accepting the preselected electronic carriers supplied by the first semiconductor pocket;

an electrically conductive gate electrode located above the

substrate and the semiconductor pockets and capable of selectively applying an electrical bias on the circuit device to control flow of the preselected electronic carriers from the first semiconductor pocket to the second semiconductor pocket; and

a curved gate layer located between the gate electrode and the semiconductor pockets to isolate the gate electrode from both the substrate and the semiconductor pockets.

62. The method as in claim 61 wherein:

the densities of the semiconductor pockets and the gate layer are within a given percentage of the substrate density;

the given percentage being selected from the group consisting of 10% and 20% whereby the integrated circuit device is resistant to accelerations, decelerations, impacts, and vibrations.

63. The method as in claim 61 wherein the gate electrode has a gate electrode material having a density which is also within the given percentage of the substrate density.

64. The method as in claim 61 wherein the integrated circuit has a field layer to electrically isolate one circuit device from a neighboring circuit device; and

the field layer consists essentially of a material having a density which is within the given percentage of the substrate density.

65. The method as in claim 64 wherein at least one of the gate and field layers are no thicker than a thickness selected from the group consisting of 0.5 microns and 10 Angstroms.